The opinion in support of the decision being entered today is *not* binding precedent of the Board

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte NEAL A. OSBORN and KENNETH D. COMSTOCK

Appeal 2007-1572
Application 09/726,831[1]
Technology Center 2600

Decided: September 27, 2007

Before JEAN R. HOMERE, JAY P. LUCAS, and MARC S. HOFF, *Administrative Patent Judges*.

HOFF, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF CASE

Appellants appeal under 35 U.S.C. § 134 from a final rejection of claims 1-13 and 15-30. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

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[1] Application filed November 30, 2000. The real party in interest is Palm Inc.

Appellants' invention relates to a system for managing display data in a computing device, particularly a personal digital assistant (PDA) or other hand-held computing device. The device includes internal and external display random access memory (RAM), and display logic which manages and allocates the internal and external display RAM according to the display mode. The display logic is configured to change the display mode during operation of the computing device (Specification 2:18-27).

Claim 1 is exemplary:

1. A computing device, comprising:

a communications bus;

a display configured to display in more than one display mode and coupled to the communications bus;

a processor, coupled to the display and to the communications bus; and

a display controller coupled to the communications bus and having dedicated internal display random access memory, the internal display random access memory being used for storing display information, the internal display random access memory configured to receive and provide access to display information to be communicated to the display, the internal display random access memory being controlled by display logic; and

a dedicated external display random access memory coupled to the display controller, the display logic being configured to manage the internal and external display random access memory and allocate the internal and external display random access memory across the internal and external display random access memory according to the display mode and the display logic is configured to change the display mode during operation

of an application running on the computing device according to changing graphical needs of the application, the display modes including at least one of resolution modes and color modes.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Reddy	US 5,712,664	Jan. 27, 1998
Nale	US 5,793,385	Aug. 11, 1998
Crocker	US 5,915,265	Jun. 22, 1999

Claims 1-13 and 15-30 stand rejected under 35 U.S.C. § 103(a) as being obvious over Crocker in view of Nale and Reddy.

Appellants contend that the Examiner erred because the limitations asserted to be taught by Reddy are not present in the reference; because the Examiner failed to articulate proper motivation or suggestion to combine the teachings of Crocker, Nale, and Reddy; and because Crocker teaches away from Reddy and from the claimed invention (Br. 8-12). The Examiner contends that Reddy teaches both internal and external display RAMs, and that the skilled artisan would have been motivated to make the combination to increase data retrieval speed and reduce on-chip power dissipation (Answer 4-5).

Rather than repeat the arguments of Appellants or the Examiner, we refer to the Briefs and the Answer for their respective details. Only those arguments actually made by Appellants have been considered in this decision. Arguments that Appellants could have made but chose not to

make in the Briefs have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii) (2004).[2]

ISSUE

The principal issue in the appeal before us is whether the Examiner erred in combining Crocker with Nale and Reddy, because Crocker contrasts its inventive system using a single memory module with the admitted prior art's use of internal and external memory devices.

FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

The Invention

1. Appellants invented a system for managing display data in a computing device having a unified memory architecture (Specification 1).

2. The memory in Appellants' device is controlled by display logic, which manages and allocates the memory according to the display mode, and is configured to change the display mode during operation of the computing device (Specification 2).

3. The display logic is operable to change the color depth of the display, or the level of resolution, or both, depending on either the

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[2] Appellants have not presented any substantive arguments directed separately to the patentability of the dependent claims or related claims in each group, except as will be noted in this opinion. In the absence of a separate argument with respect to those claims, they stand or fall with the representative independent claim. *See In re Young,* 927 F.2d 588, 590, 18 USPQ2d 1089, 1091 (Fed. Cir. 1991). *See also* 37 C.F.R. § 41.37(c)(1)(vii).

application running on the processor and/or requirements dictated by an operating system running on the processor (Specification 7).

Crocker

4. Crocker teaches dynamically sizing a dedicated memory in a shared memory buffer architecture (Abstract).

5. Crocker teaches an internal system memory 4 and an external frame buffer 6, connected to the memory controller in chipset 3 via graphics processor 5 and I/O bus 8 (Figs. 1, 2).

6. Crocker teaches a display (7) configured to display in more than one display mode and coupled to the communications bus (Fig. 1).

7. Crocker teaches that it is well known that a separate frame buffer can be coupled to the graphics controller (Fig. 1).

8. Crocker teaches that it is well known in prior art work stations to eliminate the additional cost of a stand-alone frame buffer memory unit by employing a portion of the physical system memory as the frame buffer (col. 2, ll. 25-29).

9. Crocker teaches the desirability of providing graphical support on the motherboard without requiring the expense of a corresponding add-in dedicated memory (col. 2, ll. 46-52).

Nale

10. Nale teaches an address translator for a shared memory computing system, including the ability to change display mode during operation of an application according to its changing graphical needs. A minimal amount of system memory is dedicated to the graphics controller,

and additional memory is allocated to satisfy the memory requirements of a selected graphics mode (col. 1, ll. 40-49; col. 3, ll. 13-23).

11. Nale's invention enables a system memory to be shared by a graphics controller without requiring a user to reboot the system to accommodate more demanding graphics modes (col. 1, ll. 41-44; col. 3, ll. 25-29).

Reddy

12. Reddy teaches a shared memory graphics accelerator system that provides graphics display data to a display (Abstract).

13. Reddy includes an on-chip frame buffer 112 and an off-chip frame buffer 114 (Fig. 2).

PRINCIPLES OF LAW

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a prima facie case of obviousness. *In re Piasecki*, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). The Examiner can satisfy this burden by showing some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. *KSR Int'l. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741, 82 USPQ2d 1385, 1396 (2007) (*citing In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006)). Only if this initial burden is met does the burden of coming forward with evidence or argument shift to the Appellant. *Piasecki*, 745 F.2d at 1472, 223 USPQ at 788. Thus, the Examiner must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the Examiner's conclusion.

The determination of obviousness must consider, *inter alia*, whether a person of ordinary skill in the art would have been motivated to combine the prior art to achieve the claimed invention and whether there would have been a reasonable expectation of success in doing so. *Brown & Williamson Tobacco Corp. v. Philip Morris, Inc.*, 229 F.3d 1120, 1124, 56 USPQ2d 1456, 1458-59 (Fed. Cir. 2000). *Medichem S.A. v. Rolabo S.L.*, 437 F.3d 1157, 1164, 77 USPQ2d 1865, 1869 (Fed. Cir. 2006). Where the teachings of two or more prior art references conflict, the examiner must weigh the power of each reference to suggest solutions to one of ordinary skill in the art, considering the degree to which one reference might accurately discredit another. *In re Young*, 927 F.2d 588, 591, 18 USPQ2d 1089, 1091 (Fed. Cir. 1991). If the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). Further, our reviewing court has held that:

> "A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant." *In re Gurley*, 27 F.3d 551, 553, 31 USPQ2d 1130, 1131 (Fed. Cir. 1994); *Para-Ordnance Mfg. v. SGS Importers Int'l*, 73 F.3d 1085, 1090, 37 USPQ2d 1237, 1241 (Fed. Cir. 1995), *cert. denied*, 117 S. Ct. 80 (1996).

ANALYSIS

Appellants argue that the Examiner erred in rejecting claims 1-13 and 15-30 under 35 U.S.C. § 103(a), because (a) the Examiner admits that

neither Crocker nor Nale teaches dedicated internal display RAM, dedicated external display RAM, and display logic configured to manage and allocate the two memories according to the display mode, (the display modes including at least one of resolution modes and color modes), and Reddy, asserted by the Examiner as supplying the missing teachings, fails to do so; (b) there is no suggestion to combine the teachings of Crocker, Nale, and Reddy; (c) Crocker teaches away from the teachings of Reddy, in that Crocker specifically recites moving from a prior art system including internal RAM and external RAM to a system having a single memory module; and (d) the proposed combination of Reddy and Crocker would change the principle of operation of Crocker, due to Reddy's use of two RAM modules in place of the single unified memory of Crocker.

The Examiner asserts that Crocker teaches an internal display RAM and an external display RAM, controlled by the graphics processor 5 (Answer 3:19-20; see also FF 5), but that Crocker in combination with Nale fails to explicitly teach or suggest that the memory includes an internal RAM and an external RAM for allocating between the two (Answer 4:13-15). The Examiner argues that the on-chip frame buffer 112 and off-chip frame buffer 114 of Reddy meet the limitations of internal and external display RAMs, both controlled by the graphics accelerator 110 (Answer 4: 17-18). According to the Examiner, the skilled artisan would have been motivated to make the combination in order to increase display data retrieval speed and reduce on-chip power dissipation (Answer 4:18–5:3). The Examiner asserts that Crocker does not teach away from Reddy because Crocker's Figure 1 teaches that it is well known in the art that a separate

(i.e., external) frame buffer can be coupled to the graphics controller (Answer 7:15-19).

We are persuaded by Appellants' argument that Crocker teaches away from Reddy. Crocker's Prior Art Figure 1 shows a system with (internal) system memory 4, and also (external) frame buffer 6, which is connected to the memory controller in chipset 3 via graphics controller 5 and I/O bus 8 (FF 5). Crocker explains that some prior art work stations have successfully eliminated the additional cost of a stand alone frame buffer memory unit by employing a portion of the physical system memory as the frame buffer (FF 8), but that the prior solutions have not been operating system-independent. Crocker concludes that:

> it would be desirable to be able to dynamically allocate physical memory to a device other than the operating system while maintaining the flexibility of the system to execute any arbitrary operating systems supported. Moreover, it would be desirable to provide graphical support on the motherboard without requiring the expense of a corresponding add-in dedicated memory. (FF 9; Crocker, col. 2, ll. 46-52).

We find that a person of ordinary skill, reading Crocker, would have been led to provide graphical support on the motherboard by using a single, internal RAM, employing a portion of the physical system memory as the frame buffer. Such a single RAM module implementation would be a path divergent from Reddy's teaching of internal and external RAM components, and divergent from Applicant's internal display RAM and external display RAM. Because we find that a person of ordinary skill in the art would have been led in such a divergent path by Crocker, we find that Crocker teaches

away from Reddy, and further find that the references are not properly combinable to arrive at the claimed invention.

Because Appellants have shown that the Examiner's proposed combination of references is impermissible, we will not sustain the Examiner's rejection of claims 1-13 and 15-30 under 35 U.S.C. § 103(a).

NEW GROUNDS OF REJECTION

We make the following new grounds of rejection using our authority under 37 C.F.R. § 41.50(b).

Claim 1 is rejected under 35 U.S.C. § 103(a) as being obvious over Crocker in view of Nale.

Crocker teaches a computing device (Fig. 1) comprising a communications bus (CPU bus 2 and/or I/O bus 8); a display (7) configured to display in more than one display mode and coupled to the communications bus (FF 6); a processor (1) coupled to the display and to the communications bus; a display controller (5) coupled to the communications bus and having dedicated internal display RAM (4), which is used for storing display information, and is controlled by display logic (controller 5); and a dedicated external display RAM (6) coupled to the display controller (FF 5), the display logic configured to manage the internal and external display RAM and allocate the internal and external display RAM. Crocker's Fig. 1 embodiment does not teach that the display logic is configured to change the display mode during operation of an application running on the computing device according to the changing graphical needs of the

application, the display modes including at least one of resolution modes and color modes.

Nale teaches an address translator for a shared memory computing system, including the ability to change display mode during operation of an application according to its changing graphical needs (FF 10). Nale teaches dedicating a minimal amount of system memory to the graphics controller, and dynamically allocating additional memory to the graphics controller to satisfy the memory requirements of a selected graphics mode (FF 10). Nale enables a switch to a different, "more demanding" graphics mode during operation, without the need to reboot (FF 11).

It would have been obvious to the person having ordinary skill in the art to modify Crocker to include dynamic allocation of system memory to the graphics controller to satisfy the memory requirements of a selected graphics mode, as taught by Nale, because it would have allowed the operating system to use memory space not needed by the graphics controller (for example, when only low resolution graphics are required) for other purposes (Nale, col. 1, ll. 33-38; col. 3, ll. 14-28).

Other Issues

The Board of Patent Appeals and Interferences is a review body, rather than a place of initial examination. We have made a rejection above under 37 C.F.R. § 41.50(b). However, we have not reviewed claims 2-13 and 15-30 to the extent necessary to determine whether these claims are patentable over the combination of Crocker and Nale. We leave it to the

Examiner to determine the appropriateness of any further rejections based on these references.

37 C.F.R. § 41.50(b)

37 C.F.R. § 41.50(b) provides that, "[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review."

37 C.F.R. § 41.50(b) also provides that the Appellants, *WITHIN TWO MONTHS FROM THE DATE OF THE DECISION*, must exercise one of the following two options with respect to the new grounds of rejection to avoid termination of proceedings (37 C.F.R. § 1.197 (b)) as to the rejected claims:

> (1) Reopen prosecution. Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner ...
>
> (2) Request rehearing. Request that the proceeding be reheard under 37 C.F.R. § 41.52 by the Board upon the same record ...

CONCLUSION OF LAW

We conclude that Appellants have shown the Examiner erred in rejecting claims 1-13 and 15-30. On the record before us, claims 1-13 and 15-30 have not been shown to be unpatentable.

Since we have entered a new rejection, our decision is not a final agency action.

DECISION

The Examiner's rejection of claims 1-13 and 15-30 is reversed.

We have entered a new ground of rejection against claim 1 under 37 C.F.R. § 41.50(b).

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

REVERSED

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